ABSTRACT

A method and structure for an integrated circuit comprising a substrate of a first polarity; a trench structure in the substrate; a well region of a second polarity abutting the trench structure; and a heavily doped region of the second polarity abutting the trench structure, wherein the heavily doped region is adapted to suppress latch-up in the integrated circuit, wherein the heavily doped region comprises a sub-collector region, and wherein the trench structure comprises a deep trench structure or a trench isolation structure. The integrated circuit further comprises a p+ anode in the well region and a n+ cathode in the well region, wherein the integrated circuit is configured as a latchup robust p-n diode. In another embodiment, the integrated circuit further comprises a p+ anode in the well region; a n+ cathode in the well region; and a gate structure over the p+ anode and n+ cathode.